What is Claimed is:

1. A complementary-metal-oxide-semiconductor integrated circuit comprising:

a metal-oxide-semiconductor (MOS) field-effect transistor having a source, a drain, and a gate having a gate dielectric layer; and

a bipolar transistor having an emitter, a collector, and a base, wherein the base has:

a base region with a width that separates the emitter and collector and a length, and

a base conductor that is electrically connected to the base region along its length without being blocked by intervening portions of the gate oxide layer.

2. The complementary-metal-oxide-semiconductor integrated circuit defined in claim 1 wherein the base conductor comprises doped semiconductor.

3. The complementary-metal-oxide-semiconductor integrated circuit defined in claim 1 wherein the base conductor comprises doped semiconductor patterned from a crystalline semiconductor epitaxial layer grown on the base region.

4. The complementary-metal-oxide-semiconductor integrated circuit defined in claim 1 further comprising a semiconductor substrate from which

the MOS transistor and bipolar transistor are formed, wherein the semiconductor substrate comprises a silicon-on-insulator (SOI) substrate.

5. The complementary-metal-oxide-semiconductor integrated circuit defined in claim 1 wherein:

the gate comprises a gate conductor formed on top of the gate dielectric layer from polysilicon and silicide or from metal; and

the base conductor comprises silicide.

6. A method of fabricating bipolar transistors on a complementary-metal-oxide-semiconductor integrated circuit having a semiconductor substrate; comprising:

forming a patterned base masking layer on the semiconductor substrate;

implanting ions into the substrate while the patterned base masking layer is present, wherein the base masking layer serves as an implantation mask that defines a base region in the substrate for a bipolar junction transistor; and

removing the patterned base masking layer.

7. The method defined in claim 6 wherein forming the patterned base masking layer comprises forming a patterned base masking layer on the

semiconductor substrate.

8. The method defined in claim 6 wherein the semiconductor substrate comprises a silicon-on-insulator wafer and wherein forming the patterned base masking layer comprises forming a patterned base masking layer on the silicon-on-insulator substrate.

9. The method defined in claim 6 further comprising forming a self-aligned gate for a metal-oxide-semiconductor field-effect transistor on the semiconductor substrate.

10. The method defined in claim 6 further comprising forming a patterned gate conductor layer that includes at least one doped polysilicon line or at least one metal line that is used as a metal-oxide-semiconductor field-effect transistor gate conductor of a metal-oxide-semiconductor field effect transistor gate on the semiconductor substrate and that serves as an implant mask.

11. The method defined in claim 6 further comprising forming a base conductor on top of the base region.

12. The method defined in claim 6 further comprising forming a base conductor on top of the base region by forming a patterned epitaxial silicon layer on

the base region after removing the base masking layer.

13. The method defined in claim 6 wherein forming the base masking layer comprises forming a semiconductor layer on the semiconductor substrate.

14. The method defined in claim 6 wherein forming the base masking layer comprises forming an silicon-germanium layer on the semiconductor substrate and wherein removing the base masking layer comprises etching the silicon-germanium layer, the method further comprising forming a base conductor on top of the base region after etching away the silicon-germanium layer.

15. A method of fabricating bipolar junction transistors and metal-oxide-semiconductor field effect transistors on the same integrated circuit, wherein the integrated circuit has a semiconductor substrate; comprising:

forming a metal-oxide-semiconductor transistor on the semiconductor substrate that has a source, a drain, and a gate, wherein the gate has a gate oxide layer; and

forming a bipolar junction transistor on the semiconductor substrate that has an emitter, a collector, and a base with a lightly-doped base region in the semiconductor substrate and a heavily-doped epitaxial semiconductor base conductor on top of the base region, wherein none of the gate oxide layer lies

between the heavily-doped semiconductor base conductor and the lightly-doped base region.

16. The method defined in claim 15 wherein forming the bipolar junction transistor comprises growing an epitaxial semiconductor layer from which the heavily-doped epitaxial semiconductor base conductor and portions of the source and drain are formed.

17. The method defined in claim 15 further comprising:

forming a patterned base masking layer on the substrate; and

using the base masking layer as an ion implantation mask during ion implantation into the substrate, so that the base masking layer prevents ion implantation into the lightly-doped base region.

18. A complementary-metal-oxide-semiconductor-integrated-circuit bipolar transistor on a complementary-metal-oxide-semiconductor (CMOS) integrated circuit having a semiconductor substrate, comprising:

an emitter having an emitter region in the semiconductor substrate of the CMOS integrated circuit;

a collector having a collector region in the semiconductor substrate of the CMOS integrated circuit; and

a base having:

a base region in the semiconductor substrate of the CMOS integrated circuit that lies between the emitter region and the collector region, wherein the base region has a length and a width and wherein the emitter region and the collector region are separated by the width of the base region, and

a base conductor that lies above the base region and that is electrically connected to the base region along its length, wherein the base conductor serves as a path for base current in the bipolar transistor.

19. The bipolar transistor defined in claim 18 wherein the base conductor comprises epitaxial crystalline semiconductor that is doped more heavily than the base region.

20. The bipolar transistor defined in claim 18 wherein the base conductor comprises a portion of an epitaxial silicon layer and wherein the same epitaxial silicon layer is used to form part of a source and part of a drain of a metal-oxide-semiconductor transistor.